

1000

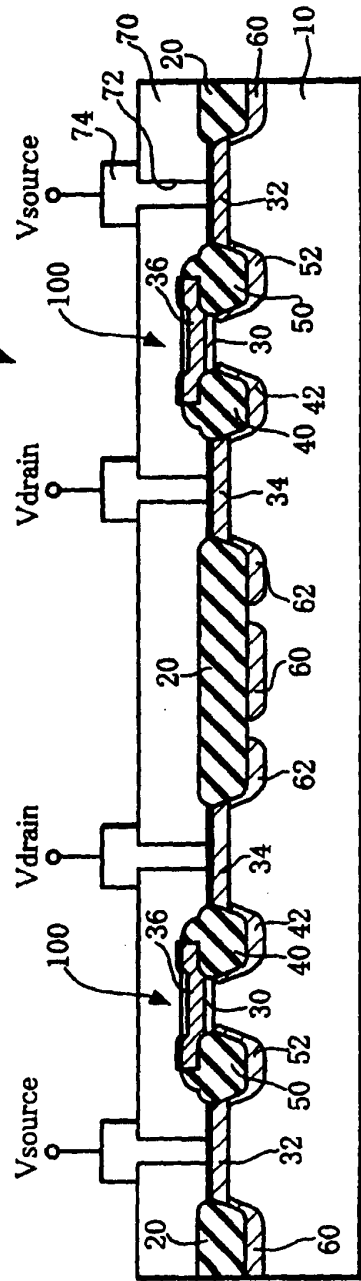


Fig. 2

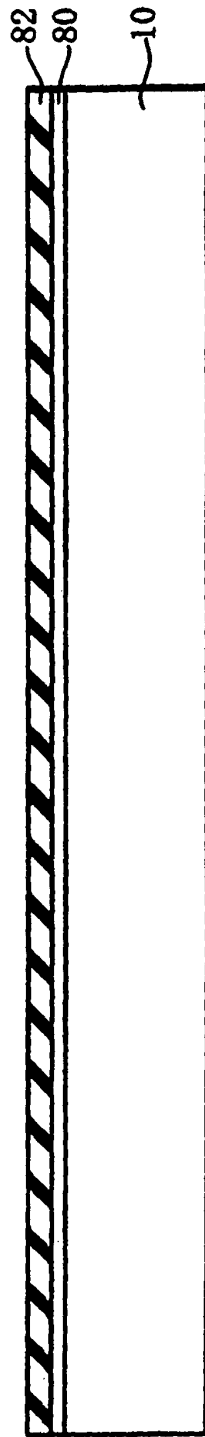
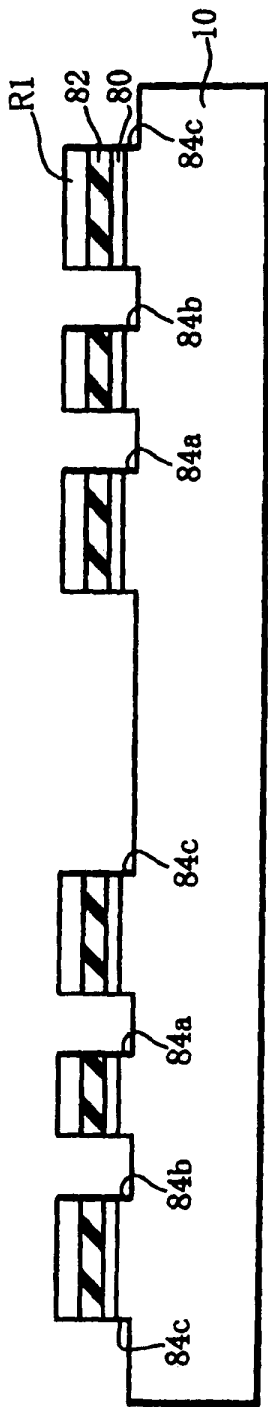


Fig. 3

(a)



(b)

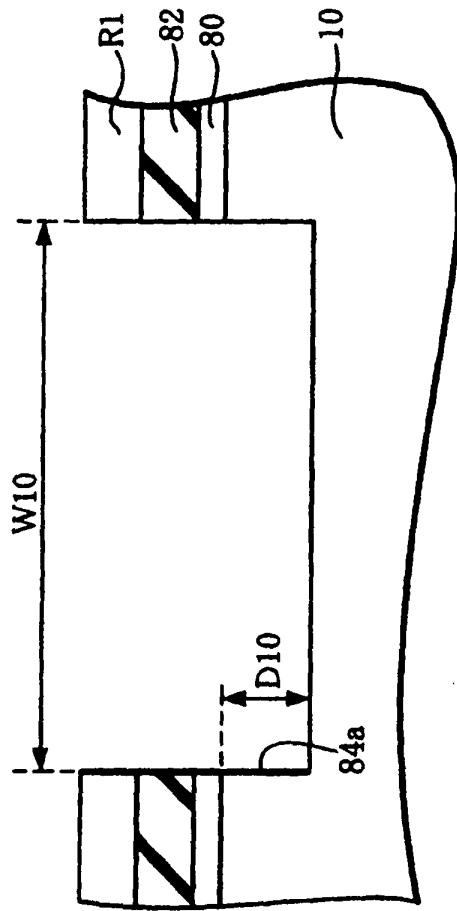
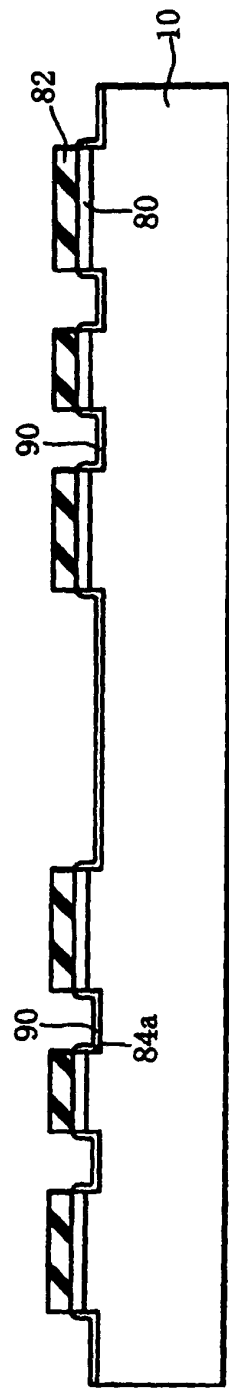


Fig. 4

(a)



(b)

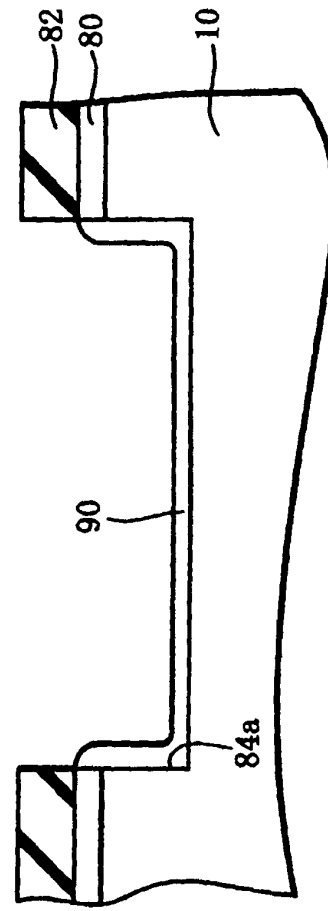


Fig. 5

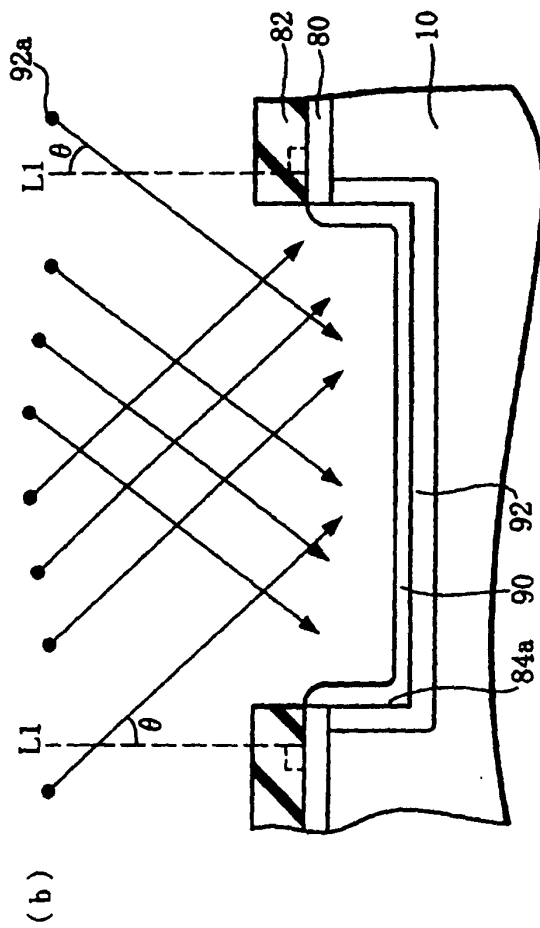
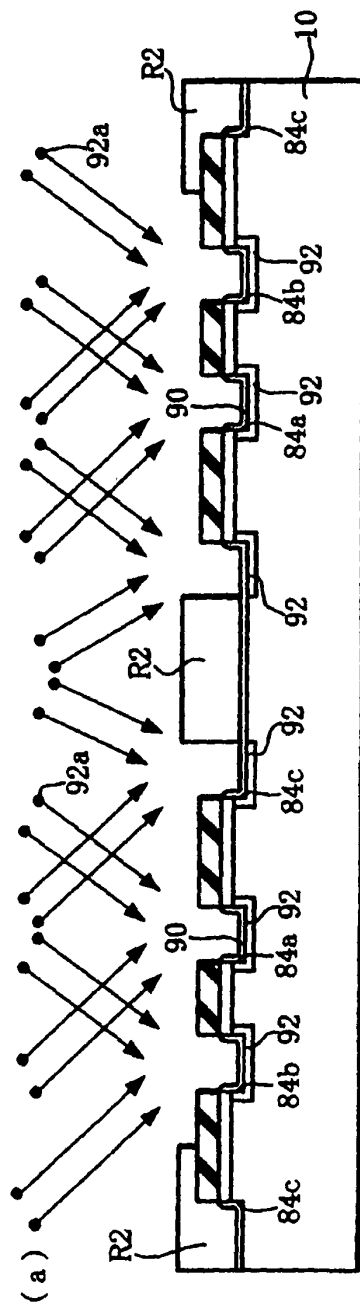


FIG. 6 is a cross-sectional view of a semiconductor device in accordance with the present invention, showing a top view of the device. The device includes a substrate 10, a gate stack 90, and a gate electrode 94. The gate stack 90 is formed on the substrate 10 and includes a gate dielectric layer 84a, a gate conductive layer 84b, and a gate capping layer 84c. The gate electrode 94 is formed on the gate stack 90 and includes a gate conductive layer 84a, a gate conductive layer 84b, and a gate capping layer 84c. The gate electrode 94 is connected to a power supply 94a. The device also includes a source/drain region 90 and a source/drain electrode 94. The source/drain region 90 is formed in the substrate 10 and includes a source/drain conductive layer 84a, a source/drain conductive layer 84b, and a source/drain capping layer 84c. The source/drain electrode 94 is formed on the source/drain region 90 and includes a source/drain conductive layer 84a, a source/drain conductive layer 84b, and a source/drain capping layer 84c. The source/drain electrode 94 is connected to a power supply 94a. The device also includes a contact region 90 and a contact electrode 94. The contact region 90 is formed in the substrate 10 and includes a contact conductive layer 84a, a contact conductive layer 84b, and a contact capping layer 84c. The contact electrode 94 is formed on the contact region 90 and includes a contact conductive layer 84a, a contact conductive layer 84b, and a contact capping layer 84c. The contact electrode 94 is connected to a power supply 94a.

Fig. 6

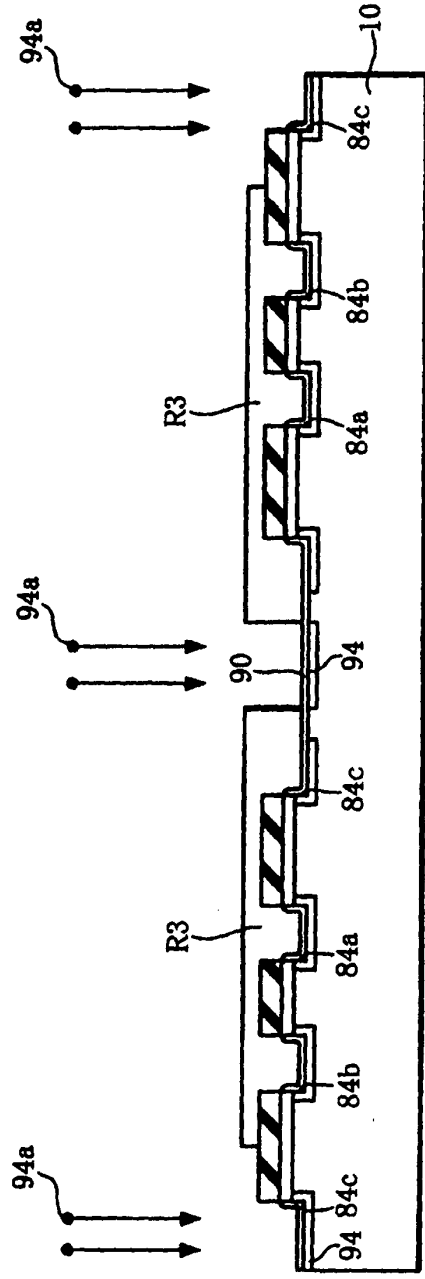
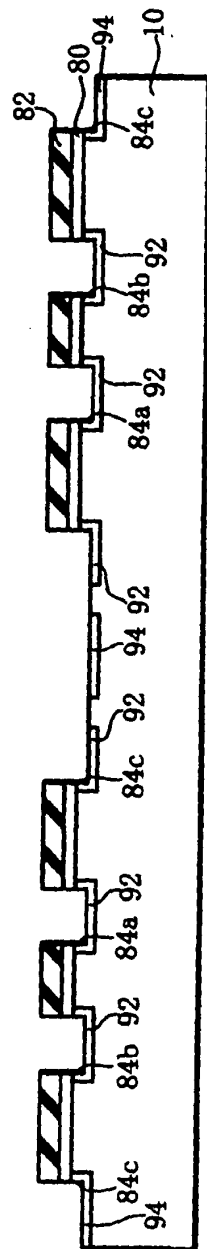


Fig. 7

(a)



(b)

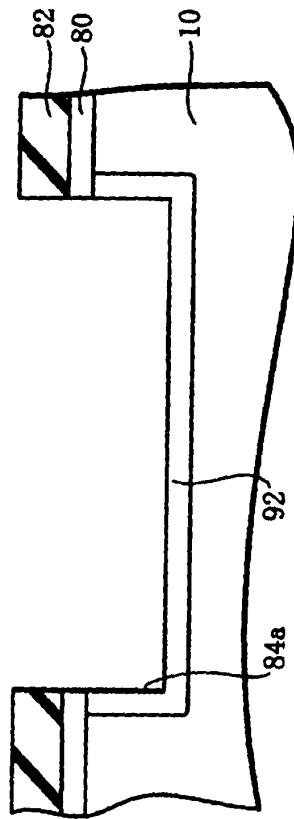
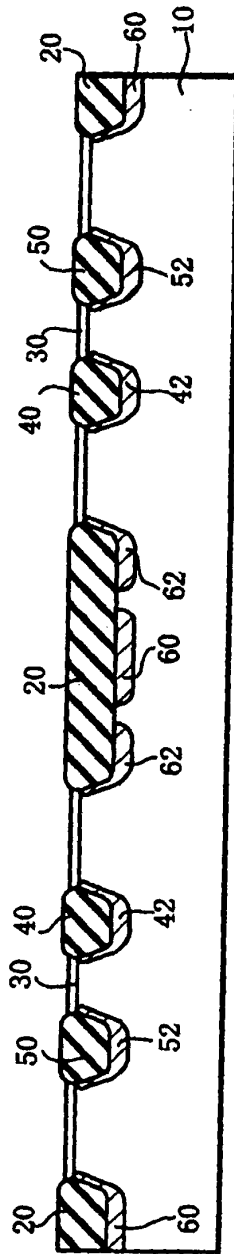


Fig. 8



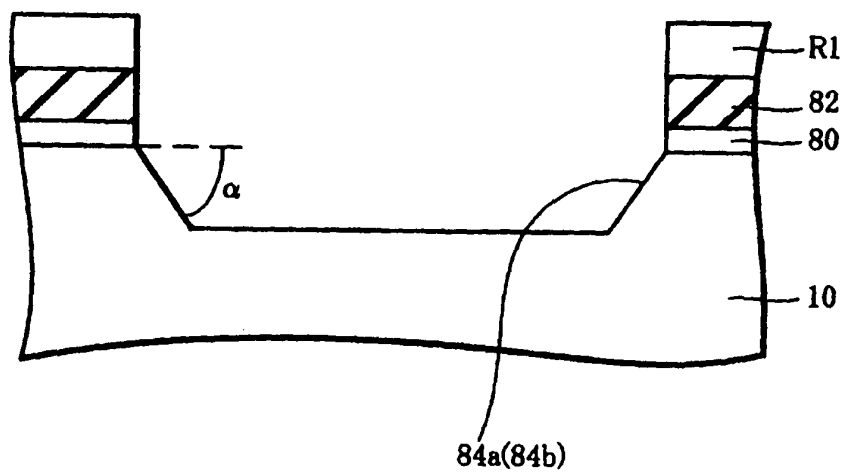


Fig. 9